

FIG. 1

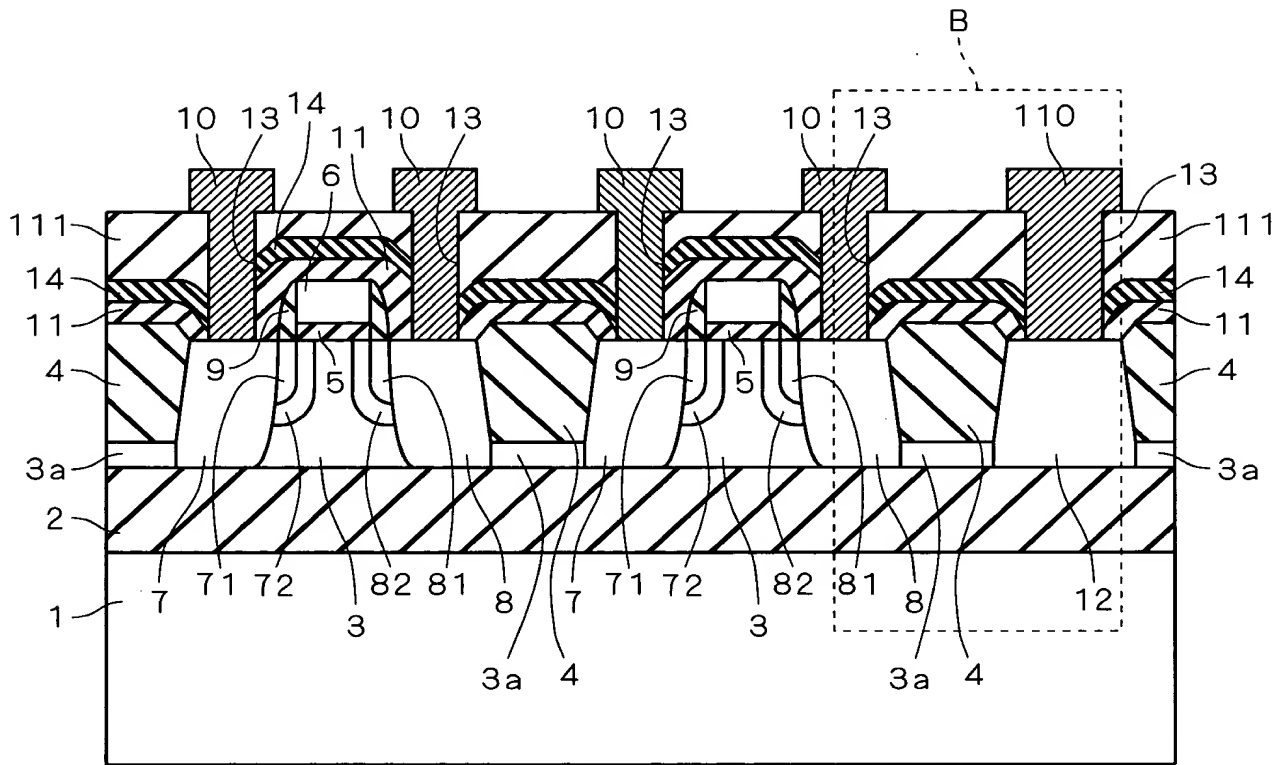


FIG. 2

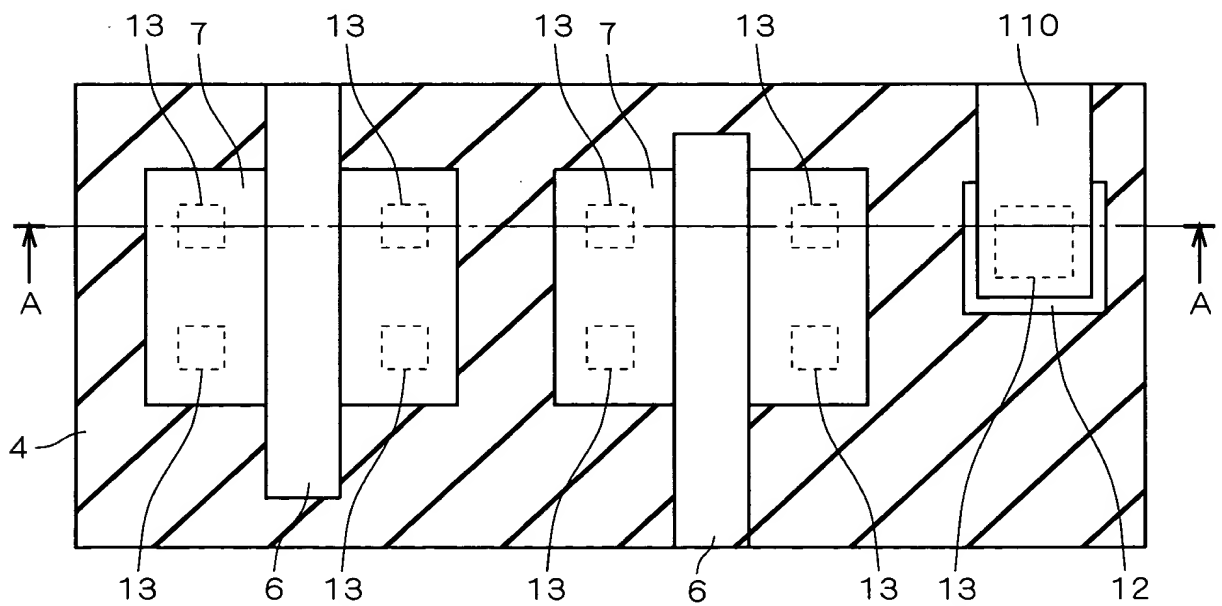
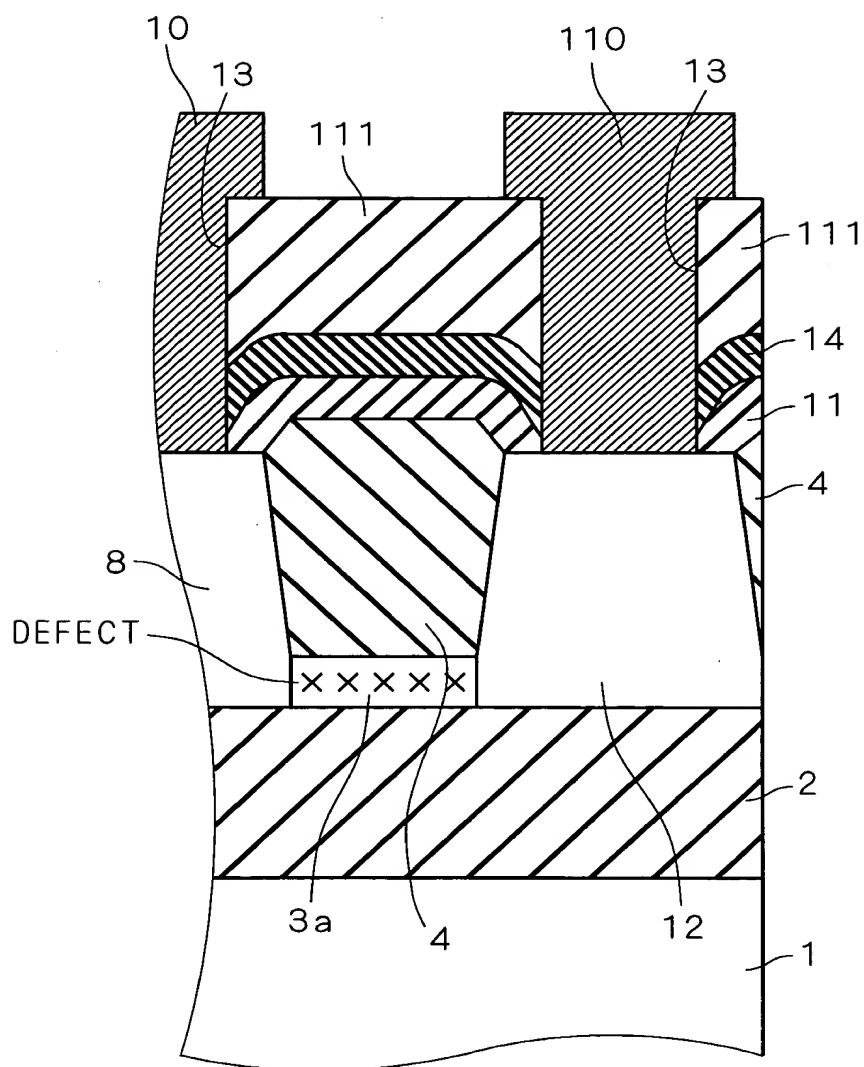


FIG. 3



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FIG. 8

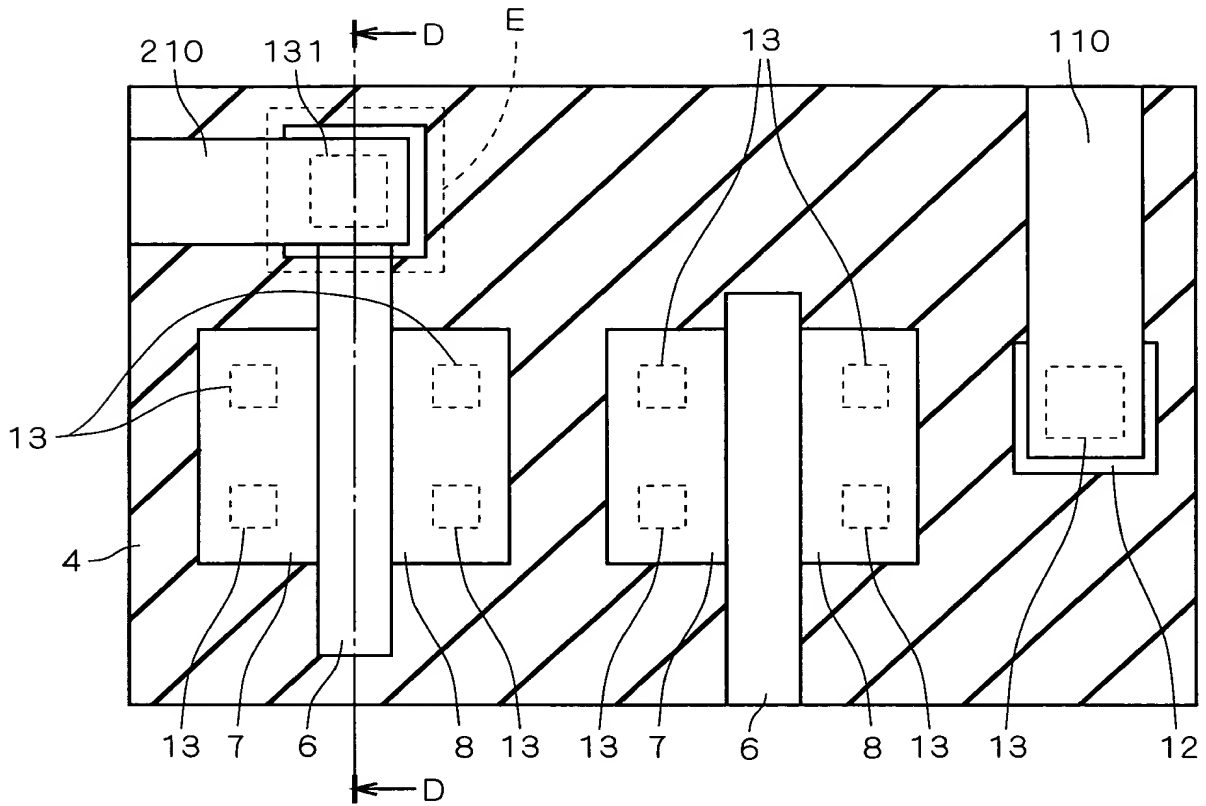
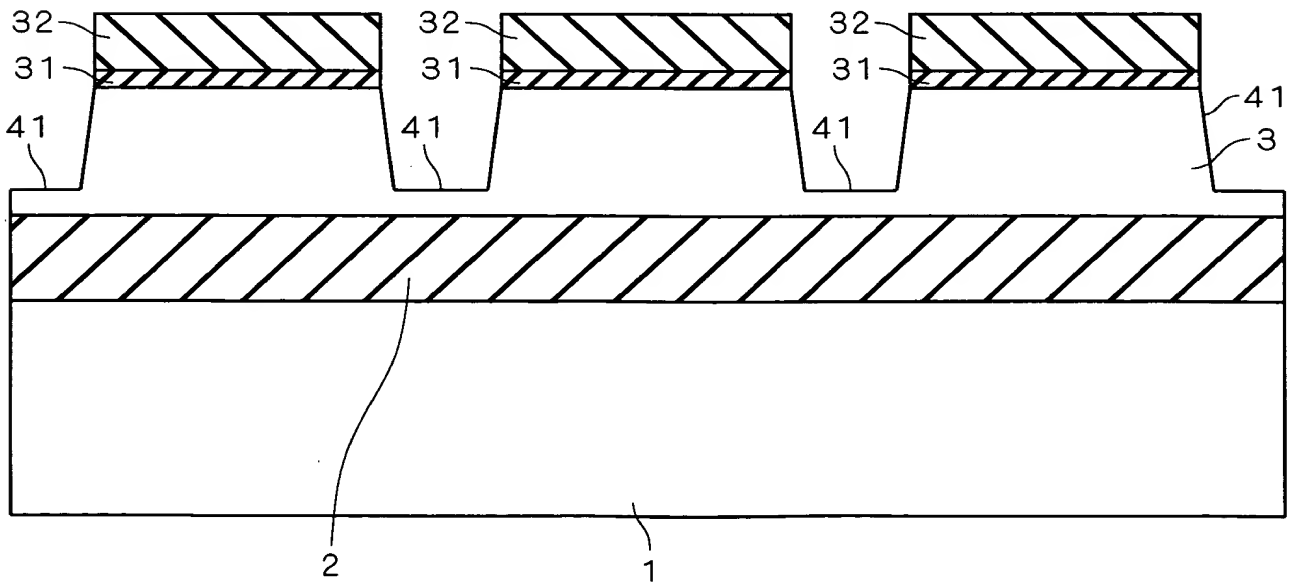


FIG. 9



[illegible]

A cross-sectional view of a multi-layered structure. The structure consists of three main layers: a top layer 1, a middle layer 2, and a bottom layer 3. Layer 2 contains a series of rectangular blocks 4. The top surface of layer 2 is labeled 3a.

This cross-sectional view shows a semiconductor device with a substrate 1 and a trench isolation structure 2. The device includes a series of gates 4 and 3a, and a series of ports 7, 71, 72, 81, 82, 8, 3, 12. The ports are connected to a common line 12. The device is shown in a cross-sectional view, with the trench isolation structure 2 separating the device into multiple sections. The gates 4 and 3a are shown as a series of rectangular blocks. The ports 7, 71, 72, 81, 82, 8, 3, 12 are shown as a series of rectangular blocks. The device is shown in a cross-sectional view, with the trench isolation structure 2 separating the device into multiple sections.

This cross-sectional view illustrates a semiconductor device with a repeating unit structure. The device is built on a substrate 1, which includes a base layer 2 and a patterned layer 3. A series of vertical pillars 4 are formed on the substrate. Each pillar 4 has a central core 5 and is surrounded by a layer 6. The pillars are connected by a horizontal layer 7. The top of the device features a series of rectangular blocks 9, which are connected by a layer 13. The device is further defined by layers 11, 14, and 302. The repeating unit is shown with a central pillar 4 and two side pillars 4, with a gap 12 between them. The labels 1, 2, 3, 3a, 4, 5, 6, 7, 71, 72, 81, 82, 9, 11, 12, 13, 14, and 302 identify the various components and layers of the device.

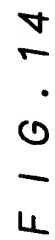


FIG. 14



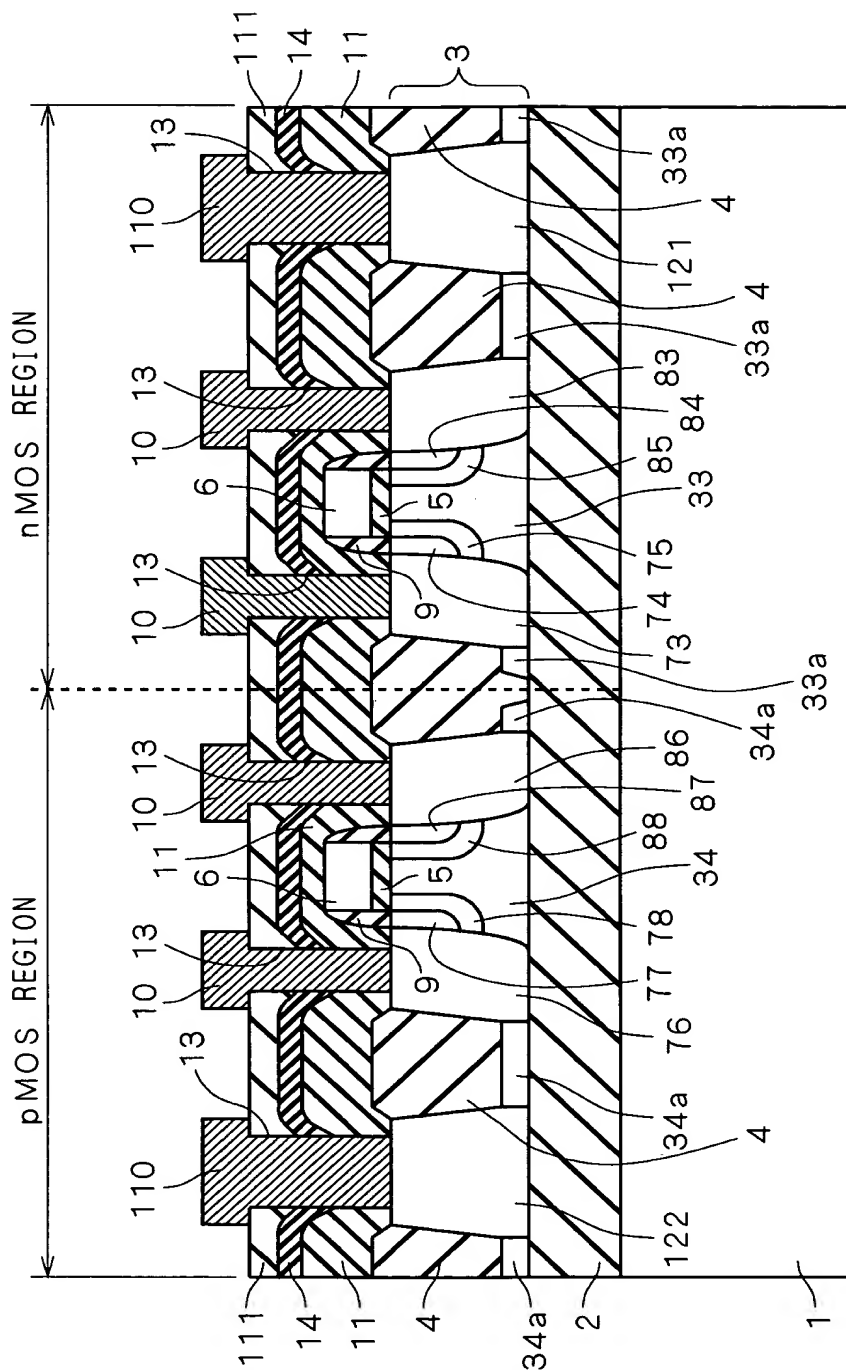


FIG. 15



FIG. 17

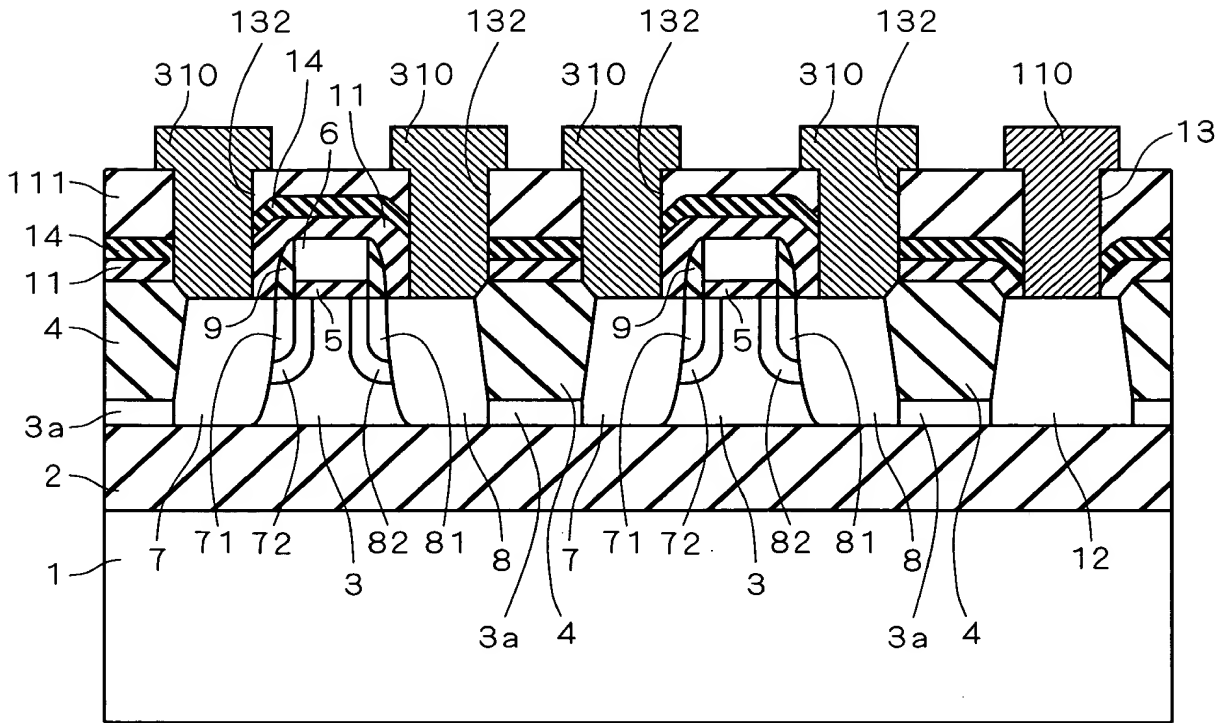
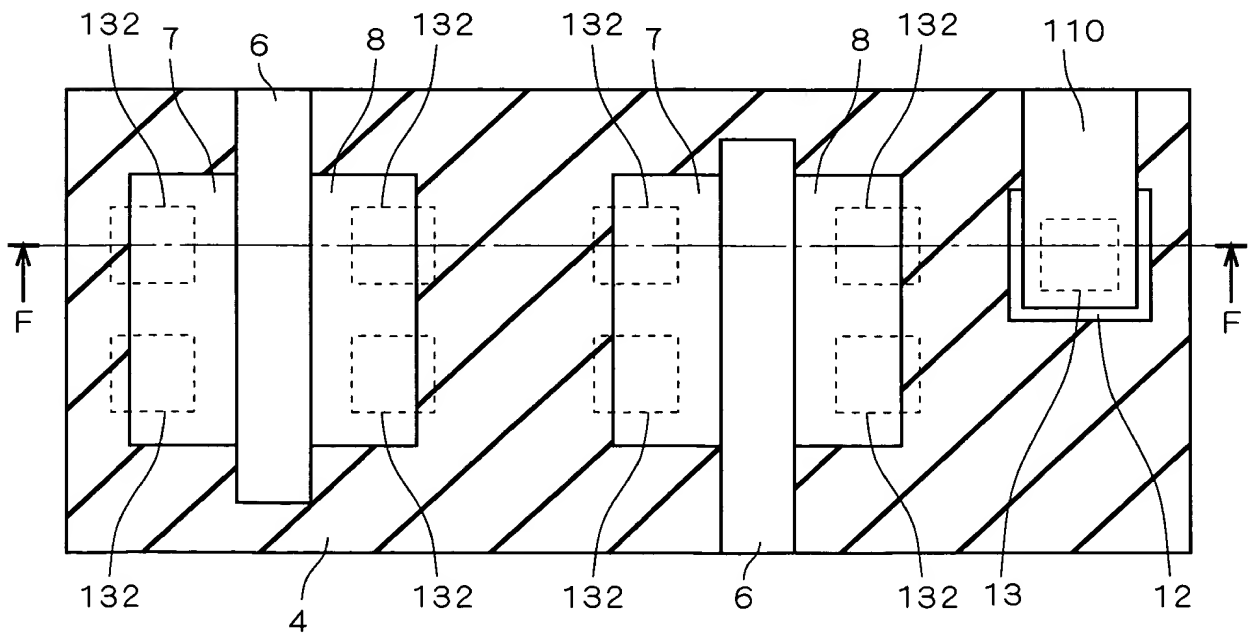


FIG. 18





This cross-sectional view shows a semiconductor device with a trench structure. The device includes a substrate (1) with a trench (2) containing a bottom layer (3a) and a top layer (3). A gate structure (4) is formed on the trench walls, and a channel layer (5) is formed on the bottom layer (3a). A contact layer (6) is formed on the top layer (3), and a contact pad (9) is formed on the contact layer (6). The device is surrounded by a passivation layer (11) and a top layer (12). The trench is defined by a trench wall (7) and a trench bottom (71, 72). The contact layer (6) is formed on the top layer (3) and the trench wall (7). The contact pad (9) is formed on the contact layer (6). The gate structure (4) is formed on the trench walls and the top layer (3). The channel layer (5) is formed on the bottom layer (3a). The bottom layer (3a) is formed on the top layer (3). The top layer (3) is formed on the substrate (1). The substrate (1) is a semiconductor material. The trench (2) is a recessed region in the substrate (1). The bottom layer (3a) is a conductive layer. The top layer (3) is a dielectric layer. The gate structure (4) is a gate oxide layer. The channel layer (5) is a channel doping layer. The contact layer (6) is a contact layer. The contact pad (9) is a contact pad. The passivation layer (11) is a passivation layer. The top layer (12) is a top layer.

FIG. 23

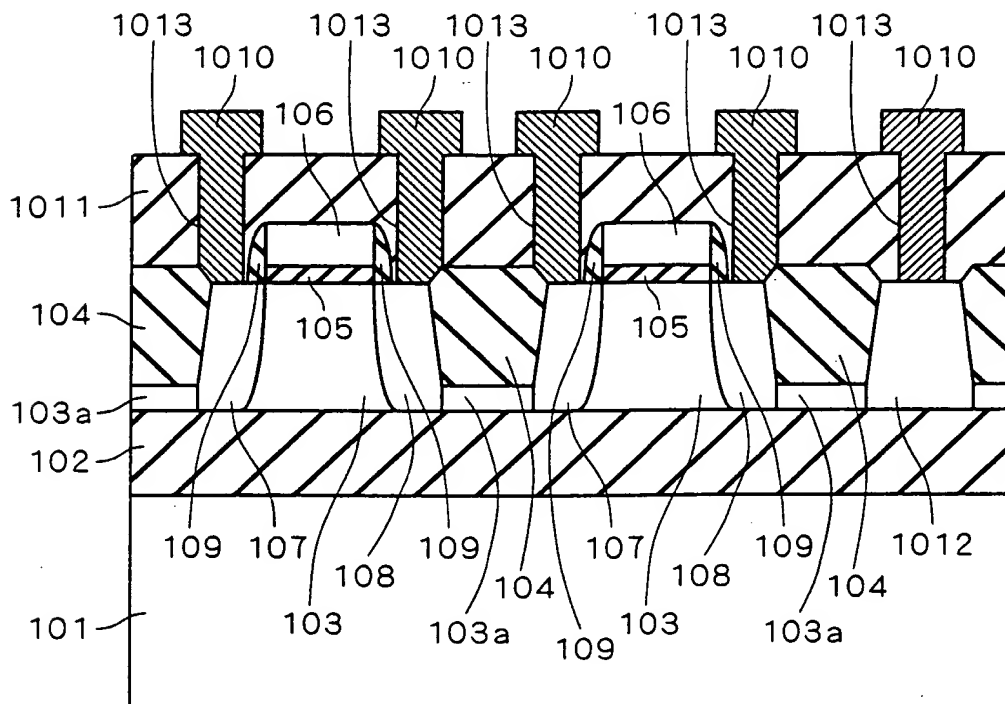


FIG. 24

